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Integrated voltage-controlled oscillator circuit using single-channel m.o.s. technology

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Abstract: A voltage-controlled oscillator (v.c.o.) circuit using single-channel m.o.s technology is described. The theory of operation of the v.c.o. is presented and the design criteria are discussed. The results obtained on the experimental integrated circuit fabricated using single-channel lateral V-m.o.s. technology show good agreement with the theory and with the results obtained from computer simulation. The circuit described results in an economical and simple v.c.o. that may be useful in a variety of applications.

1 Introduction

Two types of voltage-controlled oscillator (v.c.o.) are in common use. They are:

(*a*) harmonic oscillators[1]
(*b*) relaxation oscillators[2]

Harmonic oscillators generate nearly sinusoidal waveforms, but often require the use of inductors or large numbers of precision components and are not readily suitable for monolithic integration. Typical well known examples of these types of circuits are the Hartley, Colpits, Wien-bridge, and twin-T oscillators. Relaxation or switching oscillators are positive-feedback circuits that operate as self-triggered flip-flops. Typical examples are multivibrators and blocking oscillators. Of these, the basic multivibrator circuit is best suited for integration since it requires a minimum number of energy-storage elements (often only one capacitor) and its operation is not critically dependent upon device parameters. V.C.O.s find applications in phase-locked loops[3] in waveform generators and voltage-to-frequency convertors.

In most of the recent work,[4,5] bipolar transistors were used as active elements in voltage-controlled oscillator circuits. A v.c.o. suitable for phase-locked-loop operation using c.m.o.s. technology[6] has also been developed. At present, relatively little information is available on voltage-controlled oscillator circuits using single-channel m.o.s. technology.

The objective of this work is to present a simple integrated voltage-controlled oscillator circuit using aluminium-gate *p*-channel lateral V-m.o.s.[7*] technology and to investigate the operation of the circuit theoretically and experimentally.

The voltage-controlled oscillator circuit described can find a wide variety of applications and lead to considerable simplifications in the design and fabrication of phase-locked loops or general-purpose voltage-to-frequency convertors.

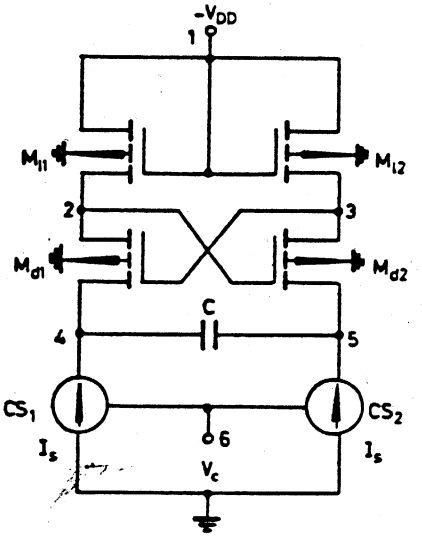

Fig. 1 *Voltage-controlled oscillator circuit*

2 V.C.O. circuit

The circuit diagram of the proposed v.c.o. is shown in Fig. 1. The circuit is similar to a bipolar version originally proposed by Grebene.[3] M_{d1} and M_{d2} are the driver transistors. The frequency-determining capacitance C is charged and discharged by two voltage (V_c) controlled current sources CS_1 and CS_2. The drains of the load transistors M_{l1} and M_{l2} are shorted to the gate, and these devices operate in the saturation region when they are on. The driver transistors M_{d1} and M_{d2} are also biased to operate in the saturation region of the characteristics.†

In the following paragraphs, the conditions for the operation of the circuit as an astable multivibrator are given. An expression for the oscillation frequency is obtained. The output-voltage waveforms as well as the limits for the linear frequency/control relationship are investigated.

* This structure is not to be confused with the double-diffused vertical V-m.o.s. structure[8] which must be used in the grounded-source configuration and which is mainly suitable for digital m.o.s. integrated circuits.

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† M_{d1} and M_{d2} can also be biased to switch between the saturation and linear regions of operation of the m.o.s.f.e.t.s, but the resulting v.c.o. does not exhibit a linear frequency/control-voltage relationship. This version of the v.c.o. is discussed in detail by Can.[9]

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The conditions for astable operation of the v.c.o. are as follows:[10]

(*a*) The d.c. operating points, when the charging capacitance C is removed, must be such that both driver transistors are in the active region.

(*b*) In this active reation, the magnitude of the loop transmission must be greater than unity at some nonzero frequency to ensure regenerative action.

(*c*) The magnitude of the loop transmission must be less than unity at d.c. to prevent bistable operation.

With the first conditions satisfied, a calculation must be made on the active region's incremental model, with the charging capacitance C short-circuited to ensure that the loop transmission is greater than unity, and with the charging capacitance removed to ensure that the loop transmission is less than unity at d.c.

The simplified analysis of the v.c.o. operation is based on the I/V characteristics derived from the simple gradual-channel approximation of the m.o.s.f.e.t. In this model, the drain current I_D for a p-channel device is given by:

(*a*) *Cut-off region*: $|V_{GS}| \leq |V_T|$

$$I_D = 0 \tag{1}$$

(*b*) *Saturation region*: $0 < |V_{GS} - V_T| \leq |V_{DS}|$

$$I_D = -\beta'(V_{GS} - V_T)^2 \tag{2}$$

(*c*) *Linear region*: $|V_{GS} - V_T| > |V_{DS}|$

$$I_D = -2\beta' \left[(V_{GS} - V_T)\, V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{3}$$

in which

$$\beta' = \frac{\mu C_0 Z}{2L} \tag{4}$$

where V_{DS} and V_{GS} are the drain-to-source and gate-to-source voltages, respectively. V_T is the threshold voltage, C_0 is the capacitance per unit area of the gate insulator. Z and L are the width and the length of the channel and μ is the carrier mobility in the channel.

Referring to Fig. 1, the operation of the circuit can be briefly explained as follows. At any given time, either M_{d1} and M_{l1} or M_{d2} and M_{l2} are conducting such that the capacitor C is alternatively charged or discharged by the constant current I_s. The voltage waveforms at nodes 2, 3, 4 and 5 are shown in Fig. 2. In this Figure, the subscripts l and d refer to the load and driver transistors, respectively, and $2\Delta V$ is the full charging voltage across the capacitor C.

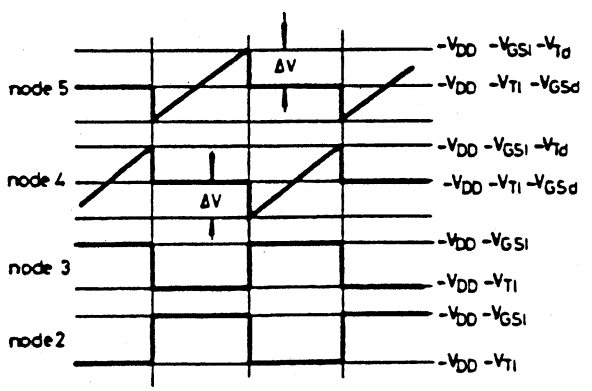

Fig. 2 *Voltage waveforms at various nodes of the v.c.o. circuit*

From an analysis of the circuit, the following relation can be obtained:

$$|\Delta V| = \sqrt{2|I_s|} \left(\frac{1}{\sqrt{\beta_l'}} - \frac{1}{\sqrt{\beta_d'}} \right) \tag{5}$$

Since the timing capacitance is charged and discharged by the voltage-controlled current source I_s during half the period T', then

$$2|\Delta V|C = |I_s| \frac{T'}{2} \tag{6}$$

Now, substituting eqn. 5 into eqn. 6, an expression for the oscillation frequency can be obtained as

$$f = \frac{\sqrt{|I_s|}}{4\sqrt{2} \left(\frac{1}{\sqrt{\beta_l'}} - \frac{1}{\sqrt{\beta_d'}} \right) C} \tag{7}$$

According to eqn. 7, for a linear voltage/frequency conversion the current supplied by the current-source transistors must be a nonlinear function of the control voltage V_c to compensate for the nonlinearity in eqn. 7. A pair of m.o.s.f.e.t.s can be used as voltage-controlled current sources (v.c.c.s.) to perform this function.

The complete v.c.o. circuit, including the voltage-controlled current source, is shown in Fig. 3.‡ For this circuit, the oscillation frequency expression becomes

$$f = \frac{\sqrt{\beta_s'}}{4\sqrt{2} \left(\frac{1}{\sqrt{\beta_l'}} - \frac{1}{\sqrt{\beta_d'}} \right) C} |V_c - V_{To}| \tag{8}$$

and can be simplified to

$$f = \frac{r_1 r_2 \beta_s'}{4\sqrt{2}(r_1 - 1)C} |V_c - V_{To}| \tag{9}$$

in which

$$r_1 = \frac{\sqrt{\beta_{dl}'}}{\sqrt{\beta_l'}} \tag{10}$$

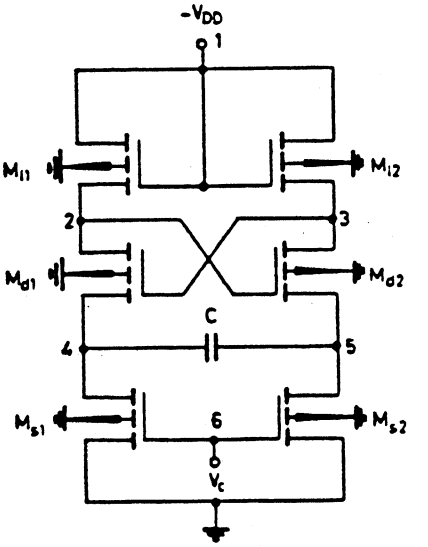

Fig. 3 *V.C.O. circuit diagram*

‡ C is an external capacitor

and

$$r_2 = \frac{\sqrt{\beta_l'}}{\sqrt{\beta_s'}} \tag{11}$$

The expression for f is obviously linear with respect to V_c.

The voltage-controlled oscillator circuit shown in Fig. 3 provides several output waveforms, such as a square wave between nodes 2 and 3, a linear ramp from nodes 4 and 5 and a triangular wave between nodes 4 and 5.

The output obtained from the drain terminal of the driver m.o.s.f.e.t. is a square wave and its high and low voltage levels V_{oH} and V_{oL} are given by

$$V_{oH} = -V_{DD} - V_{Tl} \tag{12}$$

$$V_{oL} = -V_{DD} - V_{GSl} = -V_{DD} - V_{Tl} - \frac{\sqrt{2}}{r_2}(V_c - V_{To}) \tag{13}$$

in which $V_{Tl} = V_{To} + \Delta V_{Tl}$. The lower level is a function of the control voltage V_c and the source-to-substrate bias because of the threshold V_{Tl} dependence on that voltage.

The range of control voltage V_c that yields a linear f/V_c relationship can be determined by considering the operating regions of the driver transistor M_d and the current source transistor M_s. The driver transistors operate in saturation when on, and the current source and load transistors are also saturated. To satisfy these conditions, the following equations must apply:

$$V_{To} > V_c \geq V_{To} + \frac{r_2}{\sqrt{2}} V_{Td} \tag{14}$$

$$V_{To} > V_c \geq V_{To} + \frac{r_2}{\sqrt{2} + r_2}[-V_{DD} - (V_{Tl} + V_{Td})] \tag{15}$$

3 Design and fabrication of the v.c.o.

From the above analysis of the v.c.o., the gain parameters of the current source, the load and the driver should obey the inequality $\beta_s' < \beta_l' < \beta_d'$. To achieve a high frequency of operation, β_s' should be relatively large and r_1 should be close to unity. However, making r_1 close to unity reduces the amount of regeneration. Furthermore, to obtain relatively large β_s', it is possible to choose r_2 relatively small, but this results in a reduction of the control-voltage range. In view of these facts, compromise values for r_1 and r_2 must be determined.

In the v.c.o. circuit, the current-source m.o.s.f.e.t.s must have large output resistances. It is also necessary to use large β' transistors with small internal capacitances, and it may also be desirable to employ a technology that is directly compatible with bipolar i.c. processing.

The lateral V-m.o.s. technology[7] was used for the realisation of the proposed v.c.o. It results in short channel length, low output conductance, high transconductance, small gate capacitance (and hence high cut-off frequency) and high breakdown voltages. The lateral V-m.o.s. technology is also capable of high packing density and is directly compatible with the V-groove bipolar i.c. process,[11] permitting the simultaneous fabrication of n-p-n bipolar transistors and high-speed p-channel m.o.s.f.e.t.s on the same chip.

The detailed cross-sectional structure of the aluminum gate p-channel lateral V-m.o.s.t. is shown in Fig. 4. The structure is similar to that of a standard m.o.s.f.e.t., except that the channel extends along the V-groove. The particular geometry of the V-m.o.s. offers an added advantage in controlling the reproducibility of the effective channel length and its dependence on diffusion and photolithographic parameters. In a lateral V-m.o.s.t. structure, the effective saturated channel length L' is given by

$$L' = 0{\cdot}865\, W_o - 1{\cdot}23\, x_j$$

where W_o is the width of the oxide window and x_j is the junction depth. The channel length is determined by the depth of the diffusion and the depth of the etched groove, which in turn is controlled by the width of the window opened in the oxide. Both of these dimensions can be accurately controlled to permit the fabrication of very short-channel devices with reproducible characteristics. The gate overlap capacitance is determined primarily by the area of the diffused regions exposed by the channel etch, since the unetched surface of the diffused regions is covered with a thick oxide layer. This permits the use of a relatively wide gate metallisation without increasing the overlap capacitance. Since the alignment tolerance is mainly determined by the allowable width of this gate metallisation, it is possible to fabricate short-channel devices using non-critical alignment tolerances.§

The following device parameters were chosen to satisfy a 10 μm design-layout rule as well as to obtain good device performance using the design criteria discussed. A geometrical channel width $Z_d = 500\,\mu$m was used for the driver m.o.s.f.e.t.s M_{d1} and M_{d2}. The channel length $L_d = 10\,\mu$m was used and kept constant for all the m.o.s.f.e.t.s. The other design parameters were chosen as $r_1^2 = 10$ and $r_2^2 = 10/3$, and the channel widths of the load and current source m.o.s.f.e.t.s were calculated as $Z_l = 50\,\mu$m and $Z_s = 15\,\mu$m, respectively. No attempt was made to optimise the performance of the circuit by using minimum geometries. Rather, the dimensions were chosen for ease in fabrication and subsequent testing, since the main objectives in building the integrated circuit were to check the feasibility of the design and to verify the theory of the operation of the proposed v.c.o. circuit experimentally.

The values of the significant process parameters were:

substrate type = n

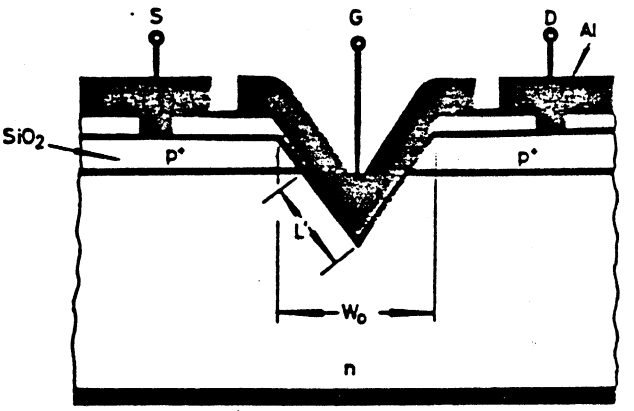

Fig. 4 *The cross-sectional structure of the p-channel lateral V-m.o.s. transistor*

§ Lateral V-m.o.s. technology can be optimised by the use of n-channel rather than p-channel devices as well as by the use of a silicon gate rather than an aluminum gate.[7]